REMARKS

This amendment is submitted in response to the office action dated September 22, 2005. Reconsideration and allowance of the claims is requested.

In this office action, claims 1, 3-6, 10-14, 16, 17, 19-21, and 23 are rejected under 35 U.S.C. 103(a) as unpatentable over *Chu* US 5,530,798 in view of *Riseman* US 4,800,442. Claims 2, 15 and 22 are rejected under 35 U.S.C. 103(a) as unpatentable over *Chu* and *Riseman*, taken further with *Morein* US 6,473,086 or *Langendorf* US 6,760,031. Finally, claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Chu* and *Riseman*, considered with *Rostoker* US 5,761,516.

In addition, claims 7-9, 18 and 24 are objected to as being dependent on a rejected claim, but otherwise considered allowable for the recitation of the swap ready I/O element and a swap ready signal.

The above rejections are respectfully traversed. The present invention, as now claimed, solves a problem not identified in the *Chu* reference, on which the Examiner basically relies, and utilizes a generated sync signal which is different from that described in the *Riseman* reference, on which the Examiner also relies.

With respect to the problem identified and solved herein, the invention relates to using multiple graphics processing units to generate separate parts of a single image. As described in [0003] of the present application, the problem that appears is of reducing synchronization issues where an image comprises a plurality of images. Reducing these effects requires a very exact synchronization system between the plural (or multiple) graphics processing units (which may not even be of identical design) to avoid the deficiencies which characterize the prior art, and which typically require very expensive solutions. As described in [0086] and [0087], and an exemplary embodiment found in figures 4E and 4F, the synchronization between the master or primary graphics unit and the secondary graphics unit encompasses generating a clock signal internally to the master unit, and correcting the phase of that clock signal to be in sync with a sync signal, and then transmitting that signal to the graphics processor of the master unit and to the secondary unit. Again in the secondary unit, the phase of the timing signal

generated in that secondary unit is compared with the phase of timing signal from the master module, and if the phases of the signals are not in sync, then the frequency of the clock generator of the slave module is adjusted to the frequency of the timing signal of the master module. Once the timing signal and the stereo field signal of each slave module are synced with the timing signal of the master GPU, then the display of the sub-images that make up the image to be displayed is allowed, resulting in a clear image.

In contrast, in the *Chu* reference on which the Examiner primarily relies, there is no detailed description of how the primary processor maintains synchronization between the primary processor and secondary processors. Further, at column 2, lines 15-30, it is disclosed that two heterogeneous graphic sync signals are generated. At line 22 it says only that the values of each picture field can be set according to a signal which is related to the vertical blanking period of the picture field since each of the graphics processors will re-synchronize themselves after ending each picture field or before beginning each picture field. The claimed invention of synchronizing the phase of a single internal to the master GPU, and then transmitting the signal from that master to the secondary GPU where the phase of an internally generated signal in that secondary GPU is matched to and synchronized with the signal received from the master GPU is not disclosed or suggested.

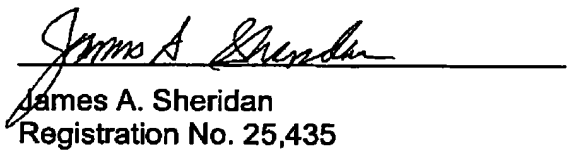
Further, that deficiency not cured by *Riseman*, nor does the Examiner suggest or allege that *Riseman* provides such a teaching. A detailed review of the newly cited *Riseman* patent finds that it is deficient in several ways. First, there is no description of the synchronization of the phase of internally generated signal to externally received signal. Further, *Riseman* relies on clock pulses being counted to establish the relative timing of the signals. *Riseman* does not disclose synchronization between a primary or master unit and secondary or a slave unit. Rather, *Riseman* only discloses generating an internal reference clock signal which is then used to clock a converter and a comparator.

Further, in *Riseman*, the apparatus is used for a laser beam printer rather than a graphical display, which means that *Riseman* does not contemplate any of the problems

appreciated or solved by the present invention. Also, since it is drawn from a different art, which the Examiner has searched only following the suggestion of the present application and claims, there is no motivation in the references themselves to adopt the *Riseman* teachings and incorporate them into the *Chu* teachings. Even if there were such a motivation (and the applicant does not concede that there is such a motivation) then the resulting combination would just generate a timing signal which is retained internal to the processing unit where the signal is generated, without contemplating transferring that signal to a secondary slave unit or comparing the phase of the transmitted signal to the phase of a signal generated internal to that secondary unit and modifying that internally generated signal.

In view of theses many distinctions, reconsideration and allowance of the claim is respectfully requested.

Respectfully submitted,



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